The Hashemite University
Electrical Engineering Department

Dr. Anas Al Tarabsheh | Digital Electronics | Date: 03/12/2008
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Q1) Fig. 1 shows a three-input ECL gate with output buffers. The transistors have the following parameters: β_F =50, V_{BE} (F.A)= 0.75V, V_{BE} (ECL)= 0.75V.

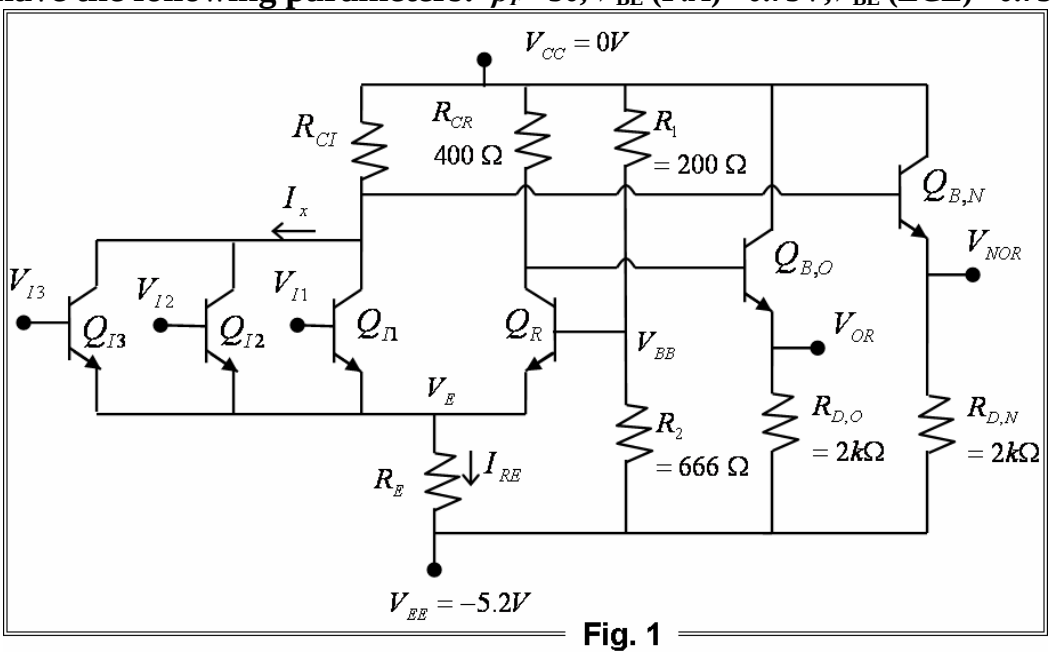

Fig. 1

A) Assuming for $V_{I1} = V_{I2} = V_{I3} = V_{IH}$, the current $I_x = 1.833mA$ and the collector-to-emitter voltage of Q_{I2} is $V_{CE2} = 1.075V$:

A.1] Determine the reference voltage V_{BB}

Hint: *if you can not solve A.1, then you are allowed to assume* $V_{BB} = -1V$ *for calculations.*

A.2] Calculate the input high-voltage V_{IH}

A.3] Find the values of R_E and R_{CI}, (*Hint: in this circuit*: $R_{CI} \neq R_{CR}$)

A.4] Calculate the output voltage V_{NOR}

A.5] Calculate the output voltage V_{OR}

B) Assuming for $V_{I1} = V_{I2} = V_{I3} = V_{IL}$:

B.1] Determine the collector-to-emitter voltage of Q_{I3} V_{CE3}

B.2] Calculate the input low-voltage V_{IL}

B.3] Determine the emitter current I_{RE}

C) Determine the average dissipated-power in the circuit $P_{EE}(avg)$

Q2) Fig. 2 shows the circuit and the corresponding load line and characteristics of a resistor loaded NMOS inverter. The NMOS inverter operates at the edge-of-saturation (EOS) as shown in Fig.2 b.

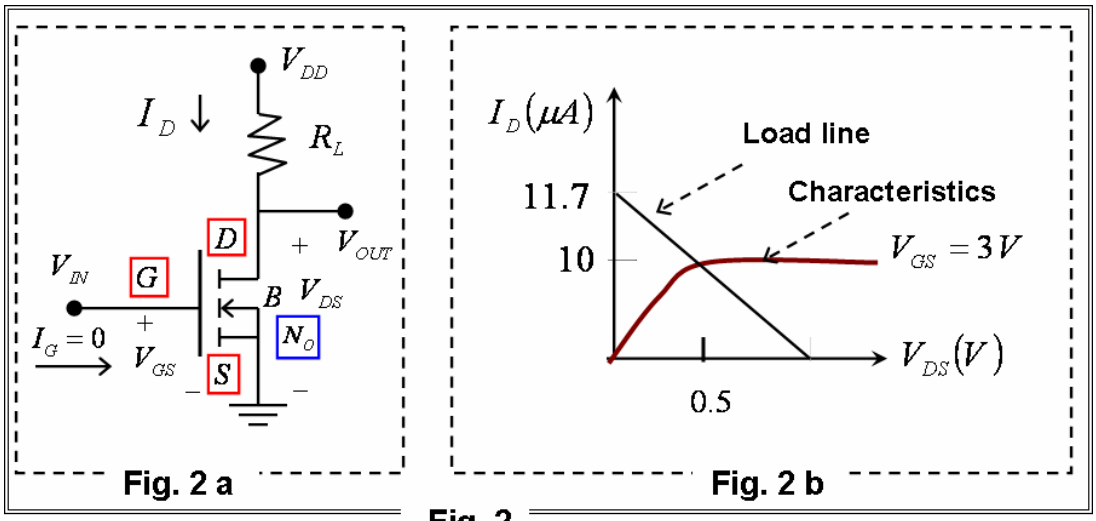

Fig. 2 a Fig. 2 b

Fig. 2

2.1) Determine the threshold voltage of the NMOS, V_{TN}.

2.2) Determine the conduction parameter of the NMOS, K_n

2.3) Calculate V_{DD} and R_L

2.4) Find the dissipated-power in the NMOS only.

2.5) Does the decrease of V_{IN} move the operating point toward the saturation region? Explain.